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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/064,474	04/22/98	ROY	TRA-040

EXAMINER

TM02/1120

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65 WOODS END ROAD
STAMFORD CT 06905

ART UNIT	PAPER NUMBER
2614	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/064,474	Subhash et al.
Examiner	**Group Art Unit**
Stacy Whitmore	2183

☒ Responsive to communication(s) filed on *Sep 6, 2000*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-21 and 24-27* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☒ Claim(s) *1-20, 26, and 27* is/are allowed.

☒ Claim(s) *21, 24, and 25* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-21, and 24-27 are presented for examination.

Claim Objections

2. Claim 21 is objected to because of the following informalities:

I. Claim 21, line 9, recites "the the processor cycle".

Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 112

3. Claims 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claims is not clearly understood:

I. As per claim 21, it is unclear exactly what is meant by "indication whether or not an instruction has been executed since a previous processor cycle". (Does this mean that information about each instruction is updated when an indication is given that an instruction has or has not been executed or does this mean that the information about each instruction is updated which includes information that an instruction has or has not been executed? explain.).

4. Claims 21, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. (6,052,774) in view of Ueki (5,428,618).

5. Segars et al. and Ueki were cited in a prior office action, dated 11/24/99.

6. As for claim 21, Segars et al. taught a method of debugging a processor, said method comprising:

providing information about processor activity in real time (col. 12, lines 59-67);

associating the instructions executed by the processor with information about processor activity (abstract),wherein

said step of providing information about processor activity includes providing information that the processor has not executed an instruction during the processor cycle (col. 13, lines 1-47).

Segars et al. did not specifically teach said step of providing information about processor activity includes providing information about every instruction executed by the processor.

However, Ueki et al. disclosed providing information about every instruction executed by said processor (see abstract, lines 11-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Segars et al. and Ueki et al. because Ueki et al.'s activity information would improve the integrity of Segars et al. system to be able to backtrack for recovering an internal state of the system (see Ueki et al., abstract).

7. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. (6,052,774) in view Ueki (5,428,618), and further in view of Folwell et al. (5,473,754).

8. Folwell et al. was cited in a prior office action, dated 11/24/99.

9. As for claims 24 and 25, Segars et al. and Ueki (5,428,618) taught the invention substantially as claimed, including the method of debugging a processor as cited in the rejection of claim 21.

Segars et al. and Ueki did not specifically teach

[24] the information about processor activity includes information as to at least one of a jump instruction has been executed, a jump instruction based on the contents of a register has been executed, a branch has been taken, and an exception has been encountered,

[25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register.

Folwell et al. taught [24] the information about processor activity includes information as to at least one of a jump instruction has been executed (col. 2, table 3), a jump instruction based on the contents of a register has been executed (col. 2, table 3), a branch has been taken (col. 2, table 2), and an exception has been encountered (col. 5, table 4), and

[25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register (col. 1, line 64 - col. 2, line 3, and col. 8, lines 1 - 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Segars et al., Ueki and Folwell et al. because having [24] information about processor activity that includes information as to at least one of a jump instruction has been executed, a jump instruction based on the contents of a register has been executed, a branch has been taken, and an exception has been encountered, [25], an indication of an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register would improve the debugging system of Segars et al. by allowing for the understanding of how program flow discontinuities are handled (Folwell et al., col. 2, lines 22-24).

10. Claims 1-20, and 26-27 are allowable over the prior art of record.

11. Applicant's arguments with respect to claims 21, filed 9/6/2000, have been fully considered but are not deemed to be persuasive.

12. In the remarks on page 4, applicant argues in substance:

A: That examiner did not cite evidence to support the reason for combination of references.

Examiner respectfully disagrees with applicant.

As to point A: Examiner cited a reason for the combination of references [see the rejection of claim 21 - "because Ueki et al.'s activity information would improve the integrity of Segars et al. system **to be able to backtrack for recovering an internal state of the system** (see Ueki et al., abstract)].

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Stacy Whitmore, whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday and alternate Fridays from 6:30AM - 4:00PM. The group fax number is (703) 306-5404.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Eddie Chan*, can be reached on *(703) 305-9712.*

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Stacy Whitmore
Nov 16, 2000

JOHN A. FOLLANSBEE
PRIMARY EXAMINER